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Production Planning and Control for Semiconductor Wafer Fabrication Facilities

Modeling, Analysis, and Systems

Springer

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Preface

Semiconductor manufacturing is one of the most important segments of the global manufacturing sector. Today semiconductor wafer fabrication facilities, for short called wafer fabs in the rest of this monograph, can be found in the USA, Europe, and Asia. Starting in the mid-1980s, the number of people in academia that deal with modeling and analysis of wafer fab operations has constantly increased. While in the beginning the number of academics working on these problems was quite small, today there are very active research groups around the world. A growing number of academics have contributed to the literature related to modeling and analysis of wafer fabs in such different areas as simulation modeling, dispatching and shop-floor scheduling, queueing models, production planning models, supply network planning models, and design and implementation of information systems for decision support. Furthermore, a wide range of other engineering models to support yield and quality improvement have been developed (cf. Chien et al. [49]). The vast academic interest in modeling and analysis of wafer fabs is caused by the fact that wafer fabs are one of the most complex and challenging industrial environments in use today.

The number of scholarly publications in this area has also increased significantly over the years. However, there are only a few survey papers that attempt to give a complete picture of various aspects of modeling and analysis of wafer fabs. The most popular among these papers are those by Uzsoy et al. [306, 307]. Except for the monographs by Atherton and Atherton [14] and Ovacik and Uzsoy [223], there are no further books in this area. The book [14] discusses modeling and analysis issues only briefly and from a different point of view. The second related book deals mainly with certain decomposition strategies based on disjunctive graphs and the shifting bottleneck heuristic for scheduling the back-end stage of semiconductor manufacturing.

In this monograph, we are interested in covering a broader area, and we attempt to take recent research trends into account. To our best knowledge, there is no book on modeling and analysis in semiconductor manufacturing that simultaneously considers production planning, production control, and the related information systems. In this book, after presenting basic concepts in the semiconductor manufacturing process and in basic modeling and analysis tools, we introduce production control schemes that are based on dispatching rules as they are predominately used in practice. Next, we discuss recent scheduling approaches. We continue with a description of order release strategies for wafer fabs. We then introduce different production planning approaches with a focus on capacity planning. In the second to last chapter, we present research related to the important field of automated material handling systems. Finally, we describe various aspects of decision support provided by manufacturing execution systems and advanced planning systems.

Based on our experience and research interests, we mainly suggest heuristics throughout the book. However, when practical, we also discuss methods that lead to optimal solutions. It is an important feature of this book that we consider discrete-event simulation in different situations as a modeling and analysis tool [89].

We have been helped by many people in the course of preparing this book. We would like to thank Cheryl Dwyer for carefully reading the entire manuscript and for providing many helpful suggestions for improvements. Ulrike Schmidt helped us by preparing parts of the figures and by checking the references. We would also like to thank Stefan Voß who strongly supported the inclusion of this book into the Springer Operations Research/Computer Science Interfaces Series.

Finally, we want to give special thanks to our friends and colleagues Oliver Rose, Stéphane Dauzère-Pérès, and Leon McGinnis. Many of the results in this monograph represent joint work with these scientists, and their insights, criticism, and support have been an important component of our research efforts. Furthermore, we also thank Reha Uzsoy, Robert C. Leachmann, Tae-Eog Lee, and Chen-Fu Chien among others for fruitful discussions that led to insights into semiconductor manufacturing and helped us to structure our knowledge on semiconductor manufacturing and finally to write this monograph.

Many people from the industry helped us with insights, datasets, and challenging problems. We especially thank Hans Ehm and Andreas Klemmt, Infineon Technologies AG; Volker Schmalfuß, X-Fab Semiconductor Foundries AG; Karl Kempf, Intel Corporation; You-In Choung, Samsung; Shekar Krishnaswamy, Applied Materials; and Detlef Pabst and Marcel Stehli, GLOBALFOUNDRIES.

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Contents

Notation

The following symbols and notation will typically be used throughout the book. We have reused some of them for several purposes due to the limited supply of symbols from the alphabet and to be consistent with papers from the literature. Their usage should be clear from the context. We also introduce additional notation when needed throughout the book.

Notation	Explanation
ACT	Average cycle time
AL	Average lateness
AT	Average tardiness
AWT	Average weighted tardiness
aux	Auxiliary resource
B	Maximum batch size
BS	Base system
BP	Base process
CDT	Carrier delivery time
C_j	Completion time of job j
$C_{\max}$	Makespan
CP	Control process
CS	Control system
CT	Cycle time
CT_j	Cycle time of job j
d_i	Individual desirability function for objective i
d_j	Due date of job j
d_{jk}	Due date for process step k of job j
D	Combined desirability function
$DU[a,b]$	Discrete uniform distribution over the integer set $\{a,\ldots,b\}$
ε	Small number or a random error $\sim N(0,\sigma^2)$
f	Number of incompatible job families
F	Number of FOUPs in a MOJ scheduling problem
$F(j)$	Family of job j
FF	Flow factor
FJm	Flexible job shop with m machine groups
h	Planning horizon
i	Machine index

Notation	Explanation
IS	Information system
j	Job index
Jm	Job shop with m machines
JS	Job processing system
k	Process step index
κ	Look-ahead parameter
L_j	Lateness of job j
$L_{\max}$	Maximum lateness
λ	(Arrival) rate
m	Number of machines
M_j	Set of machines that are possible for job j
MS	Material flow system
n	Number of jobs
n_j	Number of process steps of job j
NTJ	Number of tardy jobs
$N(\mu,\sigma^2)$	Normal distribution with mean μ and variance σ^2
O_j	Process flow of job j
O_{jk}	Operation k of job j
OS	Operational system
$\bar{p}$	Average processing time
$\mathrm{p-batch}$	Parallel batching
p_j	Processing time of job j
p_{jk}	Processing time of process step k of job j
Pm	Parallel identical machines, where the number of machines is m
PP	Planning process
PS	Planning system
recrc	Recirculation, i.e., reentrant flow
r_j	Ready time of job j
Rm	Unrelated parallel machines, where the number of machines is m
$\mathbb{R}_+$	The set of non-negative real numbers
$\mathrm{s-batch}$	Serial batching
s_{jk}	Setup time to process job k after job j
$s_{kl,ji}$	Setup time to process step l of job k after step i of job j
t	Current time
TC	Total completion time
T_j	Tardiness of job j
TP	Throughput
TT	Total tardiness
TWC	Total weighted completion time
TWT	Total weighted tardiness
τ_Δ	Planning interval
τ_{ah}	Additional planning horizon
$U(a,b)$	Continuous uniform distribution over the interval (a,b)
U_j	Indicator variable that is 1 if job j is tardy
Var(CT)	Variance of the cycle time
Var(L)	Variance of the lateness
w_j	Weight of job j
WNTJ	Weighted number of tardy jobs
x^+	$\max(x,0)$
z_i	Weight for the individual desirability function d_i
$\mathbb{Z}_+$	The set of non-negative integers